REMARKS/ARGUMENTS

Claims 1-20 remain pending in this application and stand rejected. Claims 1-3, 8-9, and 20 stand rejected under 35 U.S.C. § 101 as being non-statutory for failing to produce any real world tangible result. Claims 1-3, 8-9 and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns el al., U.S. Patent 6,819,679, (hereinafter Kerns), Sakalian et al. (U.S. Patent No. 5,056,119, hereinafter Sakalian) in view of O'Conner et al. (U.S. Patent No. 5,005,191, hereinafter O'Conner).

Claims 4-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns, Sakalian, O'Conner, in view of Wright et al. (U.S. Patent No. 7,103,049, hereinafter Wright). Claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns, Sakalian, O'Conner, in view of Mao et al. (U.S. Patent No. 7,151,773, hereinafter Mao). Claim 20 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns, Sakalian, O'Conner, in view of Taborek, Sr. et al. (US 7,020, 729, hereinafter Taborek).

The amendment to claim 1 is believed to overcome the rejections made to claims 1-3, 8-9, and 20 under 35 U.S.C. § 101. Amended claim 1 has the same scope as it had prior to being amended. The amendment to claim 1, however, clarifies the claim's language by reciting, in part, "determining the position of the synchronization pattern in the serial stream of incoming data using the selected second position." In view of the amendment to claim 1, which recites the steps for determining the position of a synchronization pattern in a serial stream of incoming data, reconsideration of the rejections of claims 1-3, 8-9 and 20 under 35 U.S.C. § 101 is respectfully requested.

Applicant submits that claim 1 is patentable over Kerns, in combination with Sakalian and O'Conner for at least the reasons cited below. Claim 1 is directed to "[a] method of determining the position of a synchronization pattern in a serial stream of incoming data." The method includes "selecting a first position from a first plurality of possible positions; testing the first selected position" and "if the first selected position is not correct, selecting a second position from a second plurality of possible positions, wherein each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit,

wherein the selected second position is used to determine the position of the synchronization pattern in the serial stream of incoming data."

As discussed earlier and agreed to by the Examiner, Kerns does not teach "selecting a first position from a first plurality of possible positions; if the first selected position is not correct, selecting a second position from a second plurality of possible positions, wherein each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit, and determining the position of the synchronization pattern in the serial stream of incoming data using the selected second position.."

The Examiner's asserts that Sakalian teaches "selecting a first position from a plurality of positions and if the selected position is not correct, selecting a second position from a second plurality of possible positions" (column 1, line 16-column 2, line 7).

The Examiner also asserts that O'Conner teaches "wherein each of the second plurality of positions shifted by one position unit wherein the selected position is used to determine the position of the synchronization pattern in the serial stream of incoming data (column 2, lines 26-42) and (column 3, lines 52-66).

Applicants respectfully disagree. As best understood, Sakalian relies on bit positions within a stream of data to determine synchronization. In column 1, lines 41-67, and column 2, lines 1-8, cited by the Examiner, Sakalian states:

"In other words, the present circuit operates on the principle that if five consecutively received bits in the selected framing bit position follow a predetermined pattern that the correct data bit position has been established. If three out of five later received bits are detected as being incorrect, (after synchronization has been established) it may be assumed that the problem is not in the selection of the wrong framing bit position, but rather in the transmission medium. If any further data bits are received in the data bit position previously selected as the framing bit position, and these bits are received with incorrect values as compared to the predetermined pattern, it may be safely assumed that a new transmission medium needs to be established and resynchronization needs to be commenced from an initial set of values. On the

other hand, if the next several framing bit positions provide the correct logic values, it may be correctly assumed that the interference problem causing the incorrect detection of logic values of data bits was a momentary occurrence and that in spite of the interference, synchronization with the transmitter has not actually been lost and thus there is no need to return to the very time consuming process of reestablishing synchronization from "scratch". As will be realized, under the worst possible conditions where there are many logic zero bit positions between framing bits, and where the framing bits alternate in logic value, it could take a large amount of time equal to the time of transmission of many data frames to establish the correct data bit position for the framing bit. Thus, it is very advantageous to temporarily return to the confirmation mode where possible, and reestablish that the correct bit position was selected and is still valid rather than returning to the selection mode to reestablish synchronization."

O'Conner, on the other hand, relies on shifting the incoming bits to determine synchronization:

"Examples of prior art circuits for establishing frame and multiframe alignment are found in U.S. Pat. No. 4,727,558, issued to Hall, and U.S. Pat. No. 4,316,284, issued to Howson. The systems described in these patents both use the same technique for establishing frame and multiframe alignment. A large shift register is used to store a portion of the received serial data stream. The shift register is tapped at 4 points which are 772 bits apart (4 frames apart), and the systems look for the 4-bit subsequences which are obtainable from the repeating 001011 pattern. A 772 bit shift register is used to hold candidate positions for frame bit positions. This shift register is shifted synchronously with data entering the large shift register. As invalid multiframe patterns are observed at the tap locations, the corresponding position out of 772 is marked in the 772 bit shift register as no longer being a valid candidate position." (2: 26-42)

"Referring to FIG. 3, serial data is input to the synchronizer on signal line 10, and shifted into a 15 frame shift register 12 at the rate of 1 bit per clock cycle. Shift register 12 holds up to 15 193-bit frames of data. 15 output taps D1-D15 are provided from the shift register 12. These taps are spaced 193 bits apart, beginning at the 193rd position from the input. These 15

taps, combined with the next data bit ready to be shifted into the register 12, identified as D0, provide 16 spaced data bits representing the most recent history of received data. D0 is the currently received bit, and D15 is the data bit received furthest in the past. Since all of the taps are spaced 193 bits apart, if D0 is actually a frame bit signaling the start of a new frame, each of the other tap data bits D1-D15 are also frame bits.: (3:52-66)

As best understood, to the extent that Sakalian looks at consecutive bits positions to determine synchronization, Sakalian teaches away from shifting the stream of bits, as required by O'Conner. Therefore, a skilled artisan applying the principles described in Sakalian is not motivated to shift the bit positions, in the manner described by O'Conner, to determine synchronization. The requisite motivation to combine Sakalian with O'Conner is lacking.

Furthermore, as best understood, it appears that combining Sakalain with O'Conner will lead to an inoperable scheme for obtaining frame synchronization. Shifting the bits, in the manner discussed in O'Conner, appears incompatible with Sakalain's attempt to determine synchronization. For example, Sakalian states:

"if five consecutively received bits in the selected framing bit position follow a predetermined pattern that the correct data bit position has been established" (Sakalian 1:42-45)

"If three out of five later received bits are detected as being incorrect, (after synchronization has been established) it may be assumed that the problem is not in the selection of the wrong framing bit position, but rather in the transmission medium. If any further data bits are received in the data bit position previously selected as the framing bit position, and these bits are received with incorrect values as compared to the predetermined pattern, it may be safely assumed that a new transmission medium needs to be established and resynchronization needs to be commenced from an initial set of values....." (Sakalian: 1:45-56)

Therefore, combining Sakalian with O'Conner, in the manner suggested by the Examiner will yield an inoperable scheme for frame synchronization. Shifting of the bits, as

shown in O'Conner has no relevance or applicability to scheme used by Sakalian to determine synchronization.

Claim 1 is thus allowable over Kerns, in view of Sakalian, and further in view of O'Conner. Claims 2-9 and 20 are dependent on claim 1 and are thus allowable for at least the same reasons as is claim 1. Claim 10-19 are allowable for at least the same reasons as is claim 1.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 752-2424.

Respectfully submitted,

Ardeshir Tabibi
Reg. No. 48,750

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
A1T:ejt
61362335 v1